DIRECTORATE OF TECHNICAL EDUCATION

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

III YEAR

M SCHEME

V SEMESTER

VERY LARGE SCALE INTEGRATION

CURRICULAM DEVELOPMENT CENTRE

M-SCHEME

(Implemented from the Academic year 2015 - 2016 onwards)

Course Name : Electronics and Communication Engineering

Subject code : 34053

Semester : V Semester

Subject Title **: VERY LARGE SCALE INTEGRATION**

TEACHING AND SCHEME OF EXAMINATION:

No of weeks per semester: 15 weeks

Subject	Instruction		Examination			
	Hrs./ Week	Hrs./ Semester	Marks			Duration
			Internal Assessment	Board Examination	Total	
Very Large Scale Integration	5	75	25	75	100	3 Hrs

Topics and Allocation of Hours:

Unit	Topic	Time (Hrs.)
I	Combinational Logic Circuits	14
II	VHDL for combinational logic circuit	13
III	Sequential Logic circuits	13
IV	VHDL for sequential Logic circuits	12
V	PLDS and FPGA circuits	11
	Test & Revision	12
	TOTAL	75

RATIONALE:

Very Large Scale integration technology, when especially used for digital integrated circuitdesign,is that it is mandatory the behaviour of the required system to be described (modelled) and verified(simulated) before synthesis tools translate the design into real hardware fabrication in the foundry(gates and wires). Hardware Description Language (HDL) allows designs to be described using any methodology - top down, bottom up or middle out. VHDL can be used to describe hardware at the gate level or in a more abstract way. This course is to introduce the digital system design concepts through hardware description Language, VHDL programming, design flow of VLSI, and architectures of CPLD and FPGA. It is mainly aimed at design of combinational and sequential functions at gate / behavioural level and simulates and verifies their functionality using the Hardware description Language (VHDL)

OBJECTIVES:

On successful completion of the course the students must be able to

- Understand device level implementation of digital gates.
- Understand the combinational circuit design and optimizing of the gate
- Design a combinational circuit for any custom made application
- Explain the building blocks for the combinational circuit
- Understand the VHDL code and circuit design process.
- Develop a VHDL code for any combinational circuit
- Answer the VHDL primitives and the importance of VHDL code in a digital circuit
- Design a digital circuit with Muxes and Encoders
- Understand the functionality of various flipflops through its excitation table.
- Design of a sequential circuit for any custom made application
- Explain the style of moore and mealy type machines
- Understand to implement VHDL code for various flipflops
- Design of sequential circuit and implementation with VHDL code
- Explain the importance of PROM, PLA, PAL and PLD
- Differentiate between the PROM,PLA and PAL.
- Develop the circuit using PROM,PAL and PLA.
- Understand the CPLD and FPGA hardware.
- Describe ASICs

VERY LARGE SCALE INTEGRATION

DETAILED SYLLABUS

Unit	Name of the Topic	Hours
I	**1.1 COMBINATIONAL CIRCUIT DESIGN:** NMOS andCMOS logic implementation of Switch, NOT, AND, OR, NAND, and NOR Gates CMOS Transmission Gate. Digital logic variable, functions, inversion, gate/circuits, Boolean algebra and circuit synthesis using gates (Up to 4 variables). **1.2 COMBINATIONAL CIRCUIT BUILDING BLOCKS**: Circuit synthesis using Multiplexer, Demultiplexer, Encoders and Decoders, Arithmetic adder, Sub tractor and Comparator circuits. Hazards and races	**7 Hrs** **7Hrs**
II	**2.1 VHDL FOR COMBINATIONAL CIRCUIT**: Introduction to VLSI and its design process. Introduction to CAD tool and VHDL: Design Entry, Synthesis, and Simulation. Introduction to HDL and different level of abstractions. HDL Statements and Assignments **2.2 VHDL CODE:** AND, OR, NAND, NOR gates, Implementation of Mux, Demux, Encoder, decoder. Four bit Arithmetic adder, sub tractor and comparator in VHDL	**8 Hrs** **5Hrs**
III	**3.1 SEQUENTIAL CIRCUIT DESIGN**: Introduction/Refreshing to Flip-flops and its excitation table, counters and Shift registers **3.2 DESIGN STEPS:** State diagram, State table, state assignment. Example for moore and mealy machines. Design of modulo counter (upto 3 bit) with only D flip-flops through state diagram	**13 Hrs**
IV	**4.1 VHDL FOR SEQUENTIAL CIRCUIT:** VHDL constructs for storage elements. VHDL code for D Latch / D, JK and T Flip-flops withorwithout reset input. **4.2 VHDL EXAMPLES**: Counters :Synchronous counters-2 bit &3 bit up counter. 3 bit up/down counter Decade counter, Johnson Counter	**5 Hrs** **7 Hrs**

V	**5 PLDS AND FPGA**: Introduction to PROM,PLA and PAL. Implementation of combinational circuits with PROM, PAL and PLA (up to 4 variables).Comparison between PROM, PAL and PLA .Introduction to Complex Programmable Logic device, Field Programmable Gate Array Introduction to ASIC. Types Of ASIC	**11 Hrs**
Revision & Test		**12 Hrs**

TEXT BOOK:

1. “Digital Design” M.Morris Mano Michael D Ciletti Pearson Education 2008

2. “Fundamentals of Digital Logic with VHDL design” Stephen brown and Vranesic 2nd edition

McGrawHill,2008

3. “VHDL Primer” Bhasker J Prentice Hall India -2009

REFERENCES:

1. “Digital Electronics with PLD Integration” Nigel P. Cook, Prentice Hall, 2000

2. “Programmable Logic Handbook: PLD, CPLD, and FPGA” Ashok K.Sharma, Mcgraw-Hill, 1998

3. “Digital Logic Simulation and CPLD Programming with VHDL” Steve Waterman Prentice Hall,